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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No. 95-0134.05		*Total Pages*	
First Named Inventor or Application Identifier			
Rich Fogal and Michael B. Ball			
Express Mail Label No.	EL003001708US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. ☒ Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. ☒ Specification *Total Pages 11* *(preferred arrangement set forth below)*
   - -Descriptive
   - -Cross References to Related Application
   - -Statement Regarding Fed sponsored R & D
   - -Reference to Microfiche Appendix
   - -Background of the Invention
   - -Brief Summary of the Invention
   - -Brief Description of the Drawings *(if filed)*
   - -Detailed Description
   - -Claim(s)
   - -Abstract of the Disclosure
3. ☒ Drawing(s) *(35 USC 113)* *Total Sheets 4* *Total Pages 12*
4. Oath or Declaration
   - a. ☐ Newly executed (original or copy)
   - b. ☒ Copy from a prior application (37CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. ☐ Computer Readable Copy
   - b. ☐ Paper Copy (identical to computer copy)
   - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☒ 37 CFR 3.73(b) Statement ☒ Power of Attorney *(where there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application Status still proper and desired
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Other

17. ☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: ____/____

18. CORRESPONDENCE ADDRESS

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Patent Application of:

Rich Fogal
Michael B. Ball

for

Angularly Offset Stacked Die Multichip Device and Method of Manufacture

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CRAIG KORENTA

Printed Name

TITLE OF INVENTION: ANGULARLY OFFSET STACKED DIE MULTICHIP DEVICE AND METHOD OF MANUFACTURE

INVENTORS: Rich Fogal, Michael B. Ball, both of Boise, ID.

ASSIGNEE: Micron Technology, Inc.

DESCRIPTION

BACKGROUND OF THE INVENTION

Technical Field. This invention generally relates to semiconductor devices. More particularly, this invention relates to a multichip module which employs stacked dice.

Background. Semiconductor devices are constructed from a silicon or gallium arsenide wafer through a process which comprises a number of deposition, masking, diffusion, etching, and implanting steps. Usually, many individual devices are constructed on the same wafer. When the devices are sawed into individual rectangular units, each takes the form of an integrated circuit (IC) die. In order to interface a die with other circuitry, normally it is mounted on a lead-frame paddle, in the case of single chip construction, or a multichip module substrate which in either case are surrounded by a number of lead fingers within a lead-frame. Hereafter general reference will be made by use of the word "substrate" as meaning either a paddle or a multichip module substrate or their functional equivalents.

The die-mounting substrate of a standard lead-frame is larger than the die itself, and it is surrounded by multiple lead fingers of individual leads. Bonding pads on the die are connected one by one in a wire-bonding operation to the lead-frame's lead finger pads with extremely fine gold or aluminum wire. The lead-frames are connected together for manufacturing purposes into a strip. Each strip generally consists of a linear series of interconnected lead-frames, typically ten in a row, one after another. Then the die and the portion of the lead-frame to which the die is attached, are encapsulated in a plastic or

ceramic material to form the chip package, as are all other die/lead-frame assemblies on the lead-frame strip. A trim-and-form operation then separates the resultant interconnected packages and bends the leads of each package into the proper configuration.

In many cases, multichip devices can be fabricated faster and more cheaply than a corresponding single IC which incorporates the same functions. Current multichip module construction typically consists of a printed circuit board substrate to which a series of separate components are directly attached. This technology is advantageous because of the increase in circuit density achieved. With increased density comes improvements in signal propagation speed and overall device weight. While integrated circuit density has and continues to increase at a significant rate, the density of the interconnecting circuitry between a die and its leads, and between two components within a multichip module, has not kept pace. Consequently, interconnection density has become a significant limiting factor in the quest for miniaturization.

U.S. Pat. No. 5,012,323, issued Apr. 30, 1991, having a common assignee with the present application, discloses a pair of rectangular integrated-circuit dice mounted on opposite sides of the lead-frame. An upper, smaller die is back-bonded to the upper surface of the lead fingers of the lead-frame via a first adhesively coated, insulated film layer. The lower, slightly larger die is face-bonded to the lower surface of the lead extensions within the lower lead-frame die-bonding region via a second, adhesively coated, insulative, film layer. The wire-bonding pads on both the upper die and the lower die are interconnected with the ends of their associated lead extensions by gold or aluminum wire. The lower die needs to be slightly larger for accessibility to the die pads from above allowing gold wire connections to the lead extensions or fingers.

U.S. Pat. No. 4,996,587 shows a semiconductor chip package which uses a chip carrier to support the chips within a cavity. The chip carrier as shown in the figures has a slot that permits connection by wires to bonding pads which, in turn, connect to the card connector by conductors. An encapsulation material is placed only on the top surface of the chip in order to provide heat dissipation from the bottom surface when carriers are stacked.

Japanese Patent No. 56-62351(A) issued to Sano in 1981 discloses three methods of mounting two chips on a lead-frame and attaching the pair of semiconductor chips or pellets to a common lead-frame consisting of: (method 1) two chips mounted on two paddles; (method 2) one chip mounted over a paddle and one below not attached to the paddle; and (method 3) one chip attached above and one chip attached below a common paddle.

U.S. Patent Nos. 5,232,060 and 5,291,061, both having a common assignee with the present application, teach arrangements of multichip stacked devices wherein a first die is attached to the substrate and wire bonded to the lead fingers, followed by a second die and so on. Both patents teach using an adhesive layer between two dice to provide clearance between the dice for the loops of the wire bonds. The wire bonds attaching an underlying die must be completed before another die can be stacked on the stack. This means that the die attachment process must be repeated for each additional layer of the stack. In addition to adding extra process steps, there is a chance of damaging the underlying wires. Additionally, because the clearances between two adjacent dice in the stack are quite tight, small variances in the loop height and adhesive thickness can lead to a compound error which results with the wire loops of the underlying die contacting or interfering with the upper die.

SUMMARY OF THE INVENTION

Accordingly, it is one object of the present invention to provide a stacked multichip device which allows at least two dice in a stack to be attached to the substrate prior to wire bonding.

Is it another object of the present invention to provide a stacked multichip device which does not restrict the loop height for the underlying die, thereby allowing thinner layers of adhesive separating the dies, facilitating ease and efficiency of wire bonding and reducing the overall height of the assembly.

In accordance with the present invention, these and other objects are achieved by an offset die stacking arrangement in connection with at least one upper level die having a width which is less than the distance separating the opposing bonding sites of the underlying die. The upper die is fixed above the lower die and rotated within a plane parallel to the lower die through an angle which insures that none of the bonding sites of the lower die are obstructed by the upper die. Dependent upon the geometries of the dice, additional dice can be stacked in this manner until the addition of an additional die would interfere with wire bonding of any of the lower dice. Once the dice are fixed in this manner, the entire assembly is subjected to the wire bonding process with all of the bonds being made in the same step. The entire process can then be repeated using the upper most die of the previous stack as the substrate.

Additional objects, advantages and novel features of the invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side view of a two die multichip device;

Fig. 2 is a top view of a first die attached to a substrate;

Fig. 3 is a top view of a first and second die attached to a substrate; and

Fig. 4 is a side view of a three die multichip device.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIGS. 1-4, a multichip device according to the invention is designated generally at reference numeral 10. Such is comprised of a conventional

substrate 12 which includes one or more Z-direction multichip stacks similar to those indicated at 14 and 16. For the purposes of this explanation, substrate 12 lies generally in the XY plain and the chip stacks extend upwardly parallel with the Z axis. However, it should be noted that the invention is not limited to this orientation and the coordinate system could describe stacks extending in the X or Y directions, as well as any other direction. Consequently, directional and position descriptors such as upper, lower, above, below, etc. are adopted merely for the convenience of illustration and explanation and are not intended to limit the orientation or scope of the invention.

Referring first to stack 14, such includes a lower first die 18 having opposed base and upper bonding surfaces 20 and 22, respectively. Base surface 20 is here adhered to substrate 12 by means of an adhesive, such as epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc. First die bonding face 22 includes a central area 24 and a plurality of bonding pads 26 which are peripheral to central area 24 and generally lie adjacent opposing side edges 27.

Multichip stack 14 also includes an upper second die 28 having opposed base and upper bonding surfaces 30 and 32, respectively. Second die bonding surface 32 includes a central area 34 and a plurality of bonding pads 36 peripheral to central area 34. A first adhesive layer 38 is interposed between and connects first die bonding surface 22 and second die base surface 30. First adhesive layer 38 is deposited within central area 24 inside of peripheral bonding pads 26.

Referring particularly to Figs. 2 and 3, upper second die 28 is angularly offset with respect to lower first die 18 at an angle which is sufficient to insure that accessibility to bonding pads 26 is not interfered with. The angular rotation of second die 28 occurs in a plane which is generally parallel to upper bonding surface 22 of first die 18. The width of upper second die 28 must be less than or equal to the perpendicular distance, W, separating opposing bonding pads 26 along opposite edges 27 of lower die 18. Constructing second die 28 with a width which is less than W allows for additional dies to be stacked without interfering with the vertical line of sight of any of the lower dies' bonding pads, thereby allowing wire bonding of all bonding sites in the same wire bonding

process step. The angle of offset, α, represents the angle between the longitudinal centerline, ℓ, of the underlying die and the longitudinal centerline, ℓ', of the overlying die. The minimum angle of offset, α, required for a die having a given opposite bonding pad separating distance, W, and an aggregate bonding pad length, L, is given by the formula

$$\alpha = \tan^{-1}\left(\frac{W}{L}\right).$$

The maximum number, N, of chips or dies of a given opposite bonding pad separating distance, W, and a given distance, L, equal to the maximum distance between the outermost two edges of the two outermost bonding sites 26 on one of sides 27, is given by the formula

$$N = \frac{180}{\tan^{-1}\left(\frac{W}{L}\right)}.$$

Table 1 below lists the approximate maximum decimal expressions of R, which are the ratios of the allowable separation distance, W, per unit length, L, for a given number of dies or chips, N.

N	R
2	1
3	.57
4	.41
5	.32
6	.26
7	.22
8	.19
9	.17

A plurality of bonding wires 44 are bonded to and between respective first die bonding pads 26 and substrate 12. Bonding wires 44 have outwardly projecting loops 46. A plurality of second bonding wires 50 are bonded to and between respective second die bonding pads 36 and substrate 12. An example of wire bonding equipment capable of

producing such wire bonds and loops is the model 1484 XQ manufactured by Kulicke and Soffa Industries Inc. of Willow Groove, PA. Wires 44 and 50 can be provided bare or be externally insulated between there respective connections to the die bonding pads and multichip module substrate.

Second multichip stack 16 is substantially similar to first stack 14, and includes a subsequent second adhesive layer 52 and third upper die 54. Thus, at least one additional adhesive layer and at least one additional die is mounted outwardly relative to the second die bonding face. Here the offset angle, α, is equal to 90° simply for ease of illustration. In this case, third die 54 is attached in a separate wire bonding step. Such third die includes a plurality of third die bonding wires 56. Third die 54 includes a central area 58 and associated peripheral bonding pads 60 which connect with third wires 56. Third die 54 can also include an overlying adhesive layer which can provide a level of additional protection to the top-most die in a multichip stack. Thus, third die 54 can be considered as an outermost chip, with second adhesive layer 52 and/or second die 28 and/or first adhesive 38 being considered as intervening material interposed between the first die bonding surface and the outermost die base surface.

While there is shown and described the preferred embodiment of the invention, it is to be distinctly understood that this invention is not limited thereto but may be variously embodied to practice within the scope of the following claims.

We claim:

1. A stacked die multichip device comprising:

a substrate;

a lower die having two opposing side edges each including bonding sites therealong, a base surface and an upper surface, the lower die being attached to the substrate with the lower die's base surface facing the substrate;

an upper die having a width less than the perpendicular distance separating any two opposing bonding sites along the opposing side edges of the lower die, this perpendicular distance being defined as W;

the upper die further having a base surface and an upper surface;

the upper die being attached above the lower die with the upper die's base surface facing the upper surface of the lower die; and

the upper die being rotated, in a plane substantially parallel to the upper surface of the lower die, through an angle sufficient to insure that no portion of the upper die interferes with a vertical line of sight of any bonding site on the lower die to permit wire bonding of the same, the upper die being fixed in this position.

2. The device of claim 1 wherein the angle of rotation for the upper die is defined as the minimum offset angle, α, and is at least equal to the value given by the formula $\alpha = \tan^{-1}(\frac{W}{L})$, where L is equal to the maximum distance between two outermost edges of any two bonding sites along one of the sides of the first die.

3. The device of claim 2 further comprising at least one additional upper die mounted on the second die in an analogous configuration as that of the second die, where the total number of dies, N, is limited by the formula $N = \frac{180}{\tan^{-1}(\frac{W}{L})}$.

4. A method for manufacturing a multichip module comprising the steps of:

affixing a lower die to a substrate, the lower die having two opposing side edges each including bonding sites therealong, a base surface and an upper surface, the lower die being attached to the substrate with the lower die's base surface facing the substrate;

orienting an upper die having a width less than the perpendicular distance separating any two opposing bonding sites along the opposing side edges of the lower die, this perpendicular distance being defined as W, the upper die further having a base surface and an upper surface, by rotating the upper die in a plane substantially parallel to the upper surface of the lower die, through an angle sufficient to insure that no portion of the upper die interferes with a vertical line of sight of any bonding site on the lower die to permit wire bonding of the same, the upper die being fixed in this position; and

attaching the upper die above the lower die with the upper die's base surface facing the upper surface of the lower die in this orientation.

5. The method of claim 4 wherein the upper die is oriented through an angle of rotation defined as the minimum offset angle, α, and is at least equal to the value given by the formula $\alpha = \tan^{-1}(\frac{W}{L})$, where L is equal to the maximum distance between two outermost edges of any two bonding sites along one of the sides of the first die.

6. The method of claim 5 further comprising attaching at least one additional upper die mounted on the second die in an analogous configuration to the attachment of the second die, where the total number of dies, N, is limited by the formula

$$N = \frac{180}{\tan^{-1}(\frac{W}{L})}.$$

ABSTRACT

An offset die stacking arrangement is disclosed having at least one upper level die having a width which is less than the distance separating the opposing bonding sites of the underlying die. The upper die is fixed above the lower die and rotated within a plane parallel to the lower die through an angle which insures that none of the bonding sites of the lower die are obstructed by the upper die. Once the dice are fixed in this manner, the entire assembly is subjected to the wire bonding process with all of the bonds being made in the same step.

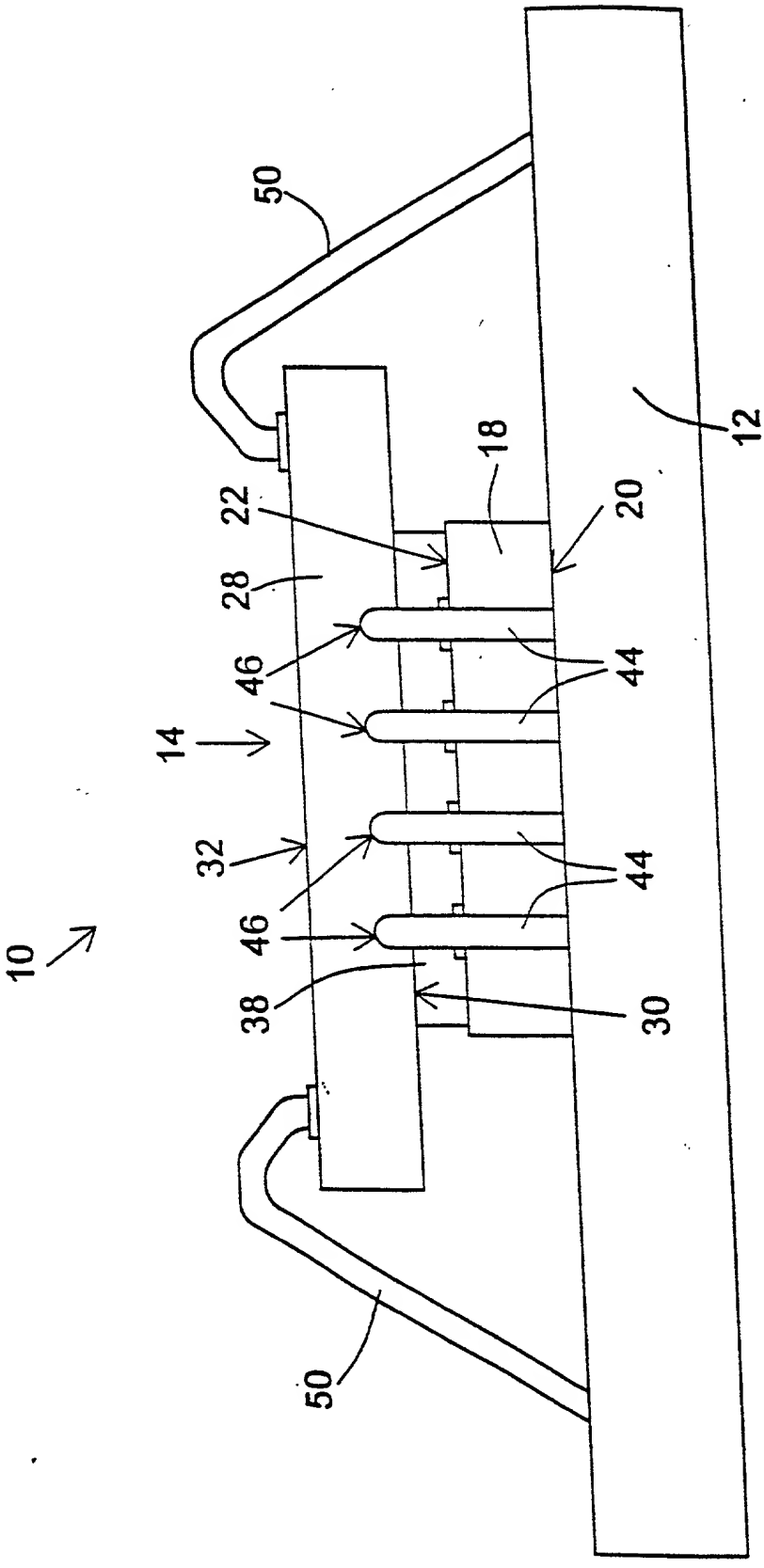

Fig. 1

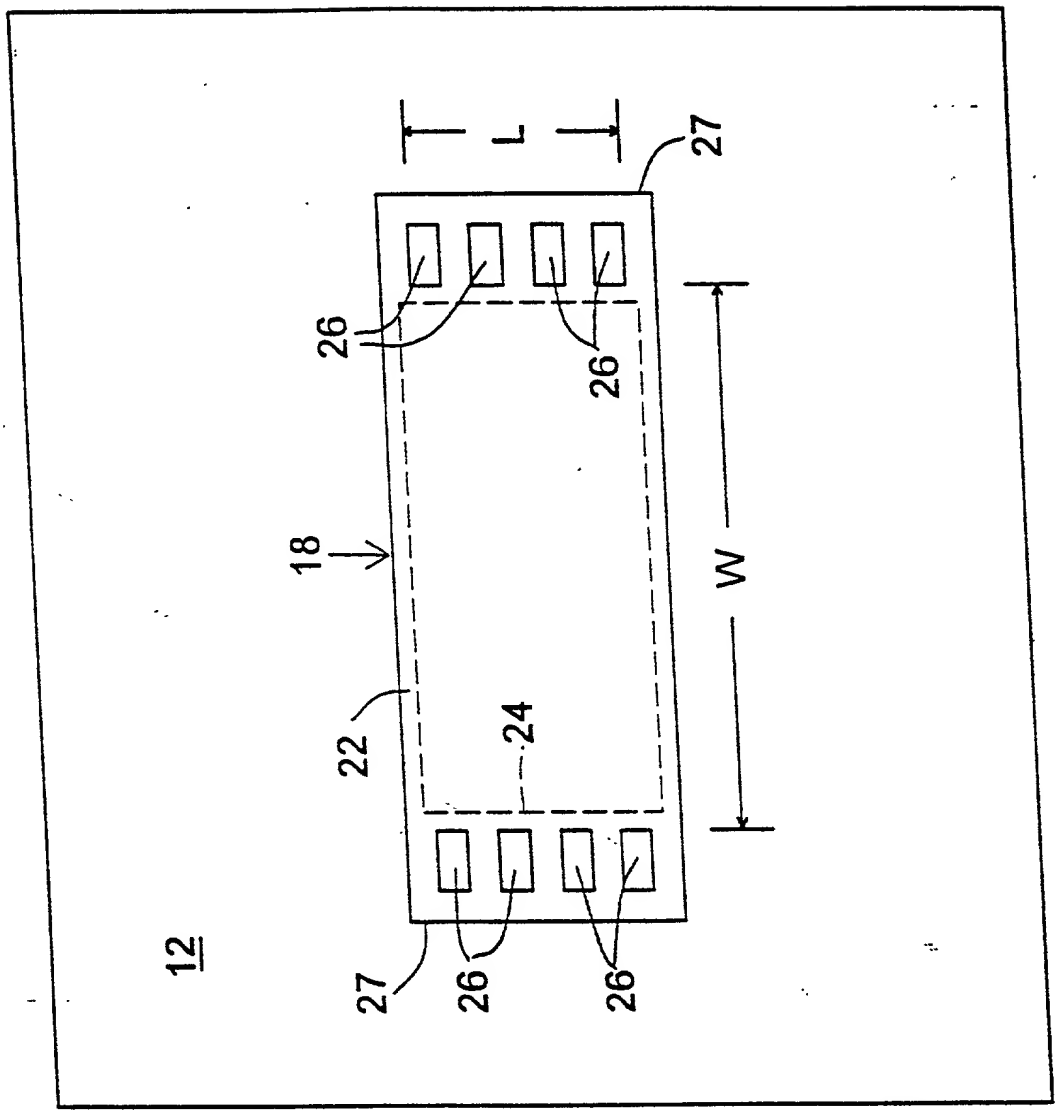

Fig. 2

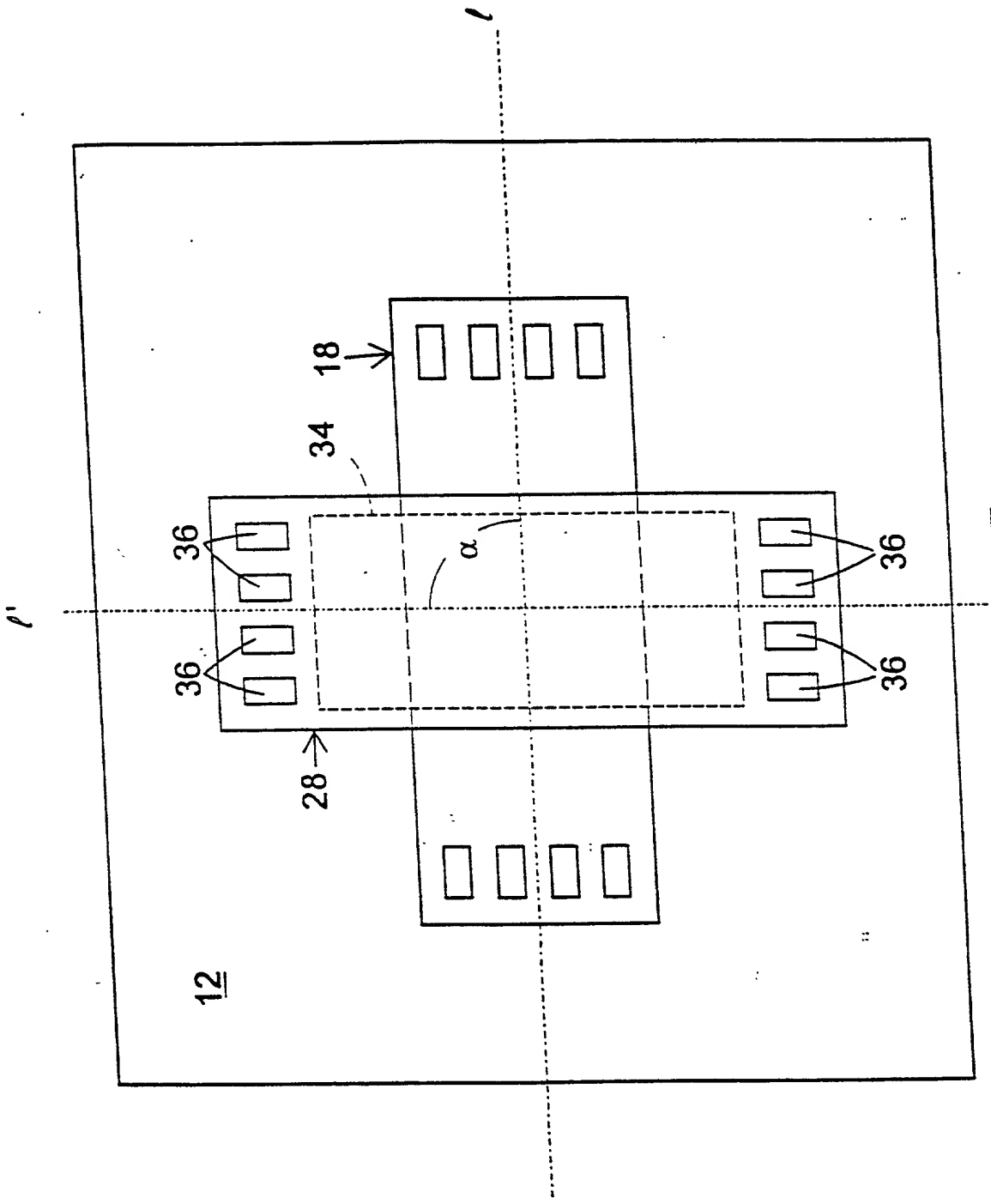

Fig. 3

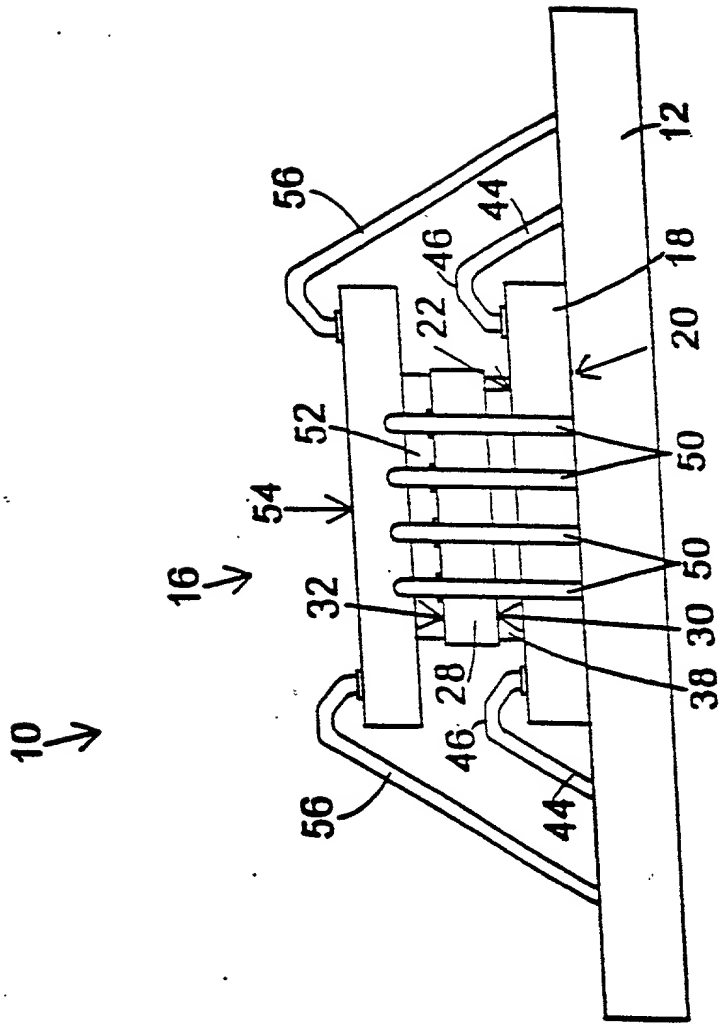

Fig. 4

DECLARATIO OR PATENT APPLICATION

ney Docket number (Optional)
M...R106 (95-0134)

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **Angularly Offset Stacked Die Multichip Device and Method of Manufacture**, the specification of which

is attached hereto unless the following box is checked:
☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.
I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

			Priority Claimed
N/A			☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	
			☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	
			☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

N/A		
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Craig M. Korfanta, Reg. No, 33,255; Lia M. Pappas, Reg. No. 34,095 and Margaret M. Dunbar, Reg. No. 37,818.
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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☐ Additional inventors are being named on separately numbered sheets attached hereto.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Rich Fogal and Michael B. Ball Serial No.: Filed: October 21, 1999 For: ANGULARLY OFFSET STACKED DIE MULTICHIP DEVICE AND METHOD OF MANUFACTURE	§ § § § § § § §	Atty. Docket: 95-0134.05 "EXPRESS MAIL" MAILING LABEL NO. EL003001708US DATE OF DEPOSIT 10-21-99 I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231. [signature] Signature

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints: Charles B. Brantley, II, Reg. No. 38,086; Michael L. Lynch, Reg. No. 30,871; Lia M. Pappas, Reg. No. 34,095; Walter D. Fields, Reg. No. 37,130; Kevin D. Martin, Reg. No. 37,882; and David J. Paul, Reg. No. 34,692 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment:

__ Filed concurrently herewith for recording, a copy of which is attached hereto.

X Previously recorded on: 8/16/95, at Reel: 7689, Frame: 0227

Please direct all communications as follows:

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ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: Oct 21, 1999

By: [signature]

Michael L. Lynch, Reg. No. 30,871
Chief Patent Counsel